

1 CLAIMS:

2 Having thus described our invention, what we claim as
3 new and desire to secure by Letters Patent is as
4 follows:

5 1. In a computer system having a processor with a
6 plurality of activity states, and at least one
7 peripheral device in operative relation with the
8 processor, a method of operating the computer system
9 comprising communicating the activity state of the
10 processor to the at least one peripheral device.

11 2. A method as recited in claim 1, further comprising:
12 supplying an interrupt from the peripheral to the
13 processor when the processor changes activity states
14 from a first activity state to a second activity state.

15 3. A method as recited in claim 2, further comprising
16 detection of the activity state of the processor by the
17 peripheral before said interrupt is supplied.

18 4. A method as recited in claim 2, wherein said
19 supplying of said interrupt is performed only if said
20 peripheral needs to be serviced by said processor.

21 5. A method as recited in claim 2, wherein the
22 peripheral has a plurality of urgency states and an
23 activity state of the processor is evaluated against

1 the urgency state of the peripheral to determine
2 whether said peripheral issues an interrupt.

3 6. A method as recited in claim 5, wherein if said
4 urgency state of said peripheral is high, said
5 peripheral issues an interrupt to said processor
6 regardless of said activity state of said processor.

7 7. A method as recited in claim 5, wherein if said
8 urgency state of said peripheral is low, said
9 peripheral issues an interrupt to said processor only
10 if said activity state of said processor is other than
11 low.

12 8. A method as recited in claim 2, wherein a plurality
13 of peripherals are in operative relation with said
14 processor, and a peripheral has issued an interrupt
15 request to said processor, the method further
16 comprises:

17 issuing interrupt requests to said processor from
18 all peripherals which need to be serviced; and

19 servicing all of said interrupt requests by said
20 processor.

21 9. A method as recited in claim 8, wherein said
22 interrupt requests are serviced by the processor before
23 the processor changes its activity state.

24 10. A method as recited in claim 8, further comprising
25 setting the urgency level of each of the peripherals

1 that have been serviced to a lowest urgency level after
2 the peripheral has been serviced.

3 11. A method as recited in claim 1, wherein the
4 activity states of the processor are represented by at
5 least one bit output of the processor.

6 12. A method as recited in claim 1, wherein the
7 activity states of the processor are represented by at
8 least one output word generated by the processor.

9 13. A method as recited in claim 1, wherein the
10 activity state of the processor is communicated as
11 being in a state selected from active, idle and sleep.

12 14. A computer system having a processor with a
13 plurality of activity states, in which interrupts from
14 at least one peripheral in operative relation with the
15 processor are serviced, the system comprising means for
16 communicating the activity state of the processor to
17 the at least one peripheral.

18
19 15. A system as recited in claim 14, further
20 comprising means for supplying an interrupt from the
21 peripheral to the processor when the processor changes
22 activity states from a first activity state to a second
23 activity state.

1 16. A system as recited in claim 15, further comprising
2 detection means associated with the peripheral for
3 detecting the activity state of the processor before
4 said interrupt is supplied.

5 17. A system as recited in claim 15, wherein said
6 means for supplying said interrupt supplies said
7 interrupt only if said peripheral needs to be serviced
8 by said processor.

9 18. A system as recited in claim 15, wherein the
10 peripheral has a plurality of urgency states, further
11 comprising means for evaluating an activity state of
12 the processor against the urgency state of the
13 peripheral to determine whether said peripheral issues
14 an interrupt.

15 19. A system as recited in claim 18, wherein if said
16 urgency state of said peripheral is high, said
17 peripheral issues an interrupt to said processor
18 regardless of said activity state of said processor.

19 20. A system as recited in claim 18, wherein if said
20 urgency state of said peripheral is low, said
21 peripheral issues an interrupt to said processor only
22 if said activity state of said processor is other than
23 low.

24 21. A system as recited in claim 14, further
25 comprising:

1 a plurality of peripherals in operative relation
2 with said processor;

3 means for said processor to receive interrupt
4 requests from all of said additional peripherals, when
5 said peripherals need to be serviced; and

6 means operatively connected with the processor for
7 servicing all of said interrupt requests.

8 22. A system as recited in claim 21, wherein said
9 means for servicing said interrupt requests services
10 said interrupt requests before the processor changes
11 its activity state.

12 23. A system as recited in claim 21, further
13 comprising:

14 means for setting the urgency level of each of the
15 peripherals that have been serviced to a lowest urgency
16 level after the peripheral has been serviced.

17 24. A system as recited in claim 14, wherein the
18 activity states of the processor are represented by at
19 least one bit output of the processor.

20 25. A system as recited in claim 14, wherein the
21 activity states of the processor are represented by at
22 least one output word generated by the processor.

23 26. A system as recited in claim 14, wherein the
24 processor has activity states selected from active,
25 idle and sleep.

1 27. A computer program product comprising a computer
2 usable medium having computer readable program code
3 means embodied therein for causing the computer to
4 effect a method for operating the computer system to
5 service interrupts from a peripheral in operative
6 relation with a processor having a plurality of
7 activity states, the method comprising communicating
8 the activity state of the processor to the at least one
9 peripheral.

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11 28. A computer program product as recited in claim 27,
12 further comprising computer readable program code means
13 embodied therein for causing the computer to supply an
14 interrupt from the peripheral to the processor, when
15 the processor changes activity states from a first
16 activity state to a second activity state.

17 29. A computer program product as recited in claim 21,
18 further comprising computer readable program code means
19 embodied therein for detecting the activity state of
20 the processor.

21 30. A computer program product as recited in claim 28,
22 further comprising computer readable program code for
23 supplying of said interrupt only if said peripheral
24 needs to be serviced by said processor.

25 31. A computer program product as recited in claim 28,
26 wherein the peripheral has a plurality of urgency

1 states, further comprising computer readable program
2 code for evaluating an activity state of the processor
3 against the urgency state of the peripheral, to
4 determine whether said peripheral issues an interrupt.

5 32. A computer program product as recited in claim 31,
6 further comprising computer readable program code which
7 if said urgency state of said peripheral is high,
8 causes said peripheral to issue an interrupt to said
9 processor regardless of said activity state of said
10 processor.

11 33. A computer program product as recited in claim 31,
12 wherein if said urgency state of said peripheral is
13 low, said peripheral issues an interrupt to said
14 processor only if said activity state of said processor
15 is other than low.

16 34. A computer program product as recited in claim 27,
17 wherein a plurality of peripherals are in operative
18 relation with said processor, and a peripheral has
19 issued an interrupt request to said processor, the
20 computer readable program code further comprises code
21 for:

22 issuing interrupt requests to said processor from
23 all peripherals which need to be serviced; and
24 servicing all of said interrupt requests by said
25 processor.

1 35. A computer program product as recited in claim 34,
2 comprising computer readable program code for servicing
3 said interrupt requests computer readable program code
4 before the processor changes its activity state.

5 36. A computer program product as recited in claim 34,
6 further comprising computer readable program code for
7 setting the urgency level of each of the peripherals
8 that have been serviced to a lowest urgency level after
9 the peripheral has been serviced.

10 37. A computer program product as recited in claim 27,
11 comprising computer readable program code wherein the
12 activity states of the processor are represented by at
13 least one bit output of the processor.

14 38. A computer program product as recited in claim 27,
15 further comprising computer readable program code
16 wherein the activity states of the processor are
17 represented by at least one output word generated by
18 the processor.

19 39. A computer program product as recited in claim 27,
20 comprising computer readable program code for detecting
21 the processor state as a state selected from active,
22 idle and sleep.

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